Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1 (currently amended): A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory;

providing a plurality of columns and rows associated with said non-volatile memory;

associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;

associating at least one spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and

enabling an error correction coding circuit during reading of said repairing data, for identifying and repairing defective columns or rows associated with said non-volatile memory despite corruption of the repairing data as read ~~to thereby identify and repair defective columns or rows associated with said non-volatile memory regardless of the corruption of said columns or rows~~.

Claim 2 (currently amended): The method of claim 1 further comprising the step of:

enabling said error correction coding circuit during an access of a main array associated with said non-volatile memory for correcting a correctable error ~~to thereby correct correctable errors~~ if a particular address corresponds to an address of at least one defective column ~~or row~~.

Claim 3 (currently amended): The method of claim 2 wherein said particular address comprises a Y-address corresponding to said at least one defective column ~~or row~~.

Claim 4 (currently amended): The method of claim 1 further comprising the step of:

~~linking a read circuit to said main array to thereby permit data to be read from said main array and transmitted to said error correction coding circuit~~ using a read circuit linked to said main array to read data from said main array and to transmit the read data to said error correction coding circuit;

~~connecting said error control circuit to said volatile latch to thereby permit data to be transferred~~ said error control circuit being connected to said volatile latch array to permit data to be transferred from said error correction coding circuit to said volatile latch array; ~~and~~

~~linking a decoder circuit to said error correction coding circuit, such that said decoder circuit is linked to said information array, at least one spare row, and said main array, wherein~~ said error correction coding circuit being linked to a decoder circuit and thereby to said information array, at least one spare row and said main array, and wherein said main array includes a normal array and at least one spare column.

Claim 5 (currently amended): The method of claim 4 further comprising the step of:

~~linking said volatile latch to said decoder circuit to thereby permit data~~ contained within said volatile latch array to be accessed by said decoder circuit.

Claim 6 (currently amended): The method of claim 1 further where in the step of reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory~~,~~ further comprises the steps of:

accessing said repairing data contained within said information array following initialization of a computer system associated with said non-volatile memory; and

thereafter transferring said ~~column~~ repairing data to said non-volatile memory.

Claim 7 (currently amended): A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory;

providing a plurality of columns and rows associated with said non-volatile memory;

associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;

associating a spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and

enabling an error correction coding circuit during an access of a main array associated with said non-volatile memory ~~to thereby correct correctable errors~~ for correcting a correctable error ~~if~~ at a particular address corresponds to an address of at least one defective column ~~or row~~, wherein said particular address comprises a Y-address ~~corresponding to said at least one defective column or row~~.

Claim 8 (currently amended): A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, wherein said ~~column repair~~ repairing data is read utilizing a read circuit linked to a main array associated with said non-volatile memory and an error correction coding circuit linked to said volatile latch array and thereby to a decoder circuit;

providing a plurality of columns and rows associated with said non-volatile memory;

associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;

associating a spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and

enabling said error correction coding circuit during an access of said main array for correcting a correctable error ~~to thereby correct correctable errors~~ if a particular address corresponds to an address of at least one defective column ~~or row~~, wherein said particular address comprises a Y-address ~~corresponding to said at least one defective column or row~~.

Claim 9 (currently amended): A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, wherein said column repair data is read utilizing a read circuit linked to a main array associated with said non-volatile memory and an error correction coding circuit linked to said volatile latch array and thereby to a decoder circuit;

providing a plurality of columns and rows associated with said non-volatile memory;

associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;

associating a spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and

enabling said error correction coding circuit during reading of said repairing data to thereby identify and repair defective columns ~~or rows~~ associated with said non-volatile memory despite ~~regardless of the~~ corruption of ~~said columns or rows~~ the repairing data as read.

Claim 10 (currently amended): A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory following initialization of a computer system associated with said non-volatile memory, wherein said column repair data is read utilizing a read circuit linked to a main array associated with said non-volatile memory and an error correction coding circuit linked to said volatile latch array and thereby to a decoder circuit;

providing a plurality of columns and rows associated with said non-volatile memory;

associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;

associating a spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and

enabling said error correction coding circuit during reading of said repairing data to thereby identify and repair defective columns ~~or rows~~ associated with said non-volatile memory despite ~~regardless of the~~ corruption of ~~said columns or rows~~ the repairing data as read.

Claim 11 (currently amended): A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a reading circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory;

providing a plurality of columns and rows associated with said non-volatile memory;

associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;

associating a spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and

an error correction coding circuit enabled during reading of said repairing data for identifying and repairing defective columns or rows associated with said non-volatile memory despite corruption of the repairing data as read ~~to thereby identify and repair defective columns or rows associated with said non-volatile memory regardless of the corruption of said columns or rows~~.

Claim 12 (currently amended): The system of claim 11 further comprising :

said error correction coding circuit enabled during an access of a main array associated with said non-volatile memory for correcting a correctable error ~~to thereby correct correctable errors~~ if a particular address corresponds to an address of at least one defective column ~~or row~~.

Claim 13 (currently amended): The system of claim 12 wherein said particular address comprises a Y-address corresponding to said at least one defective column ~~or row~~.

Claim 14 (currently amended): The system of claim 11 further wherein ~~comprising:~~

said read circuit is linked to said main array to thereby permit data to be read from said main array and to be transmitted to said error correction coding circuit;

said error control circuit is connected to said volatile latch array to thereby permit data to be transferred from said error correction coding circuit to said volatile latch array; and

~~a decoder circuit linked to~~ said error correction coding circuit~~, such that said decoder circuit~~ is linked to a decoder circuit, and thereby to said information array, at least one spare row, and said main array, said main array includes a normal array and at least one spare column.

Claim 15 (currently amended): The system of claim 14 further wherein ~~comprising:~~

said volatile latch array is linked to said decoder circuit to thereby permit data contained within said volatile latch array to be accessed by said decoder circuit.

Claim 16 (currently amended): The system of claim 11 wherein:

said repairing data contained within said information array is accessed following initialization of a computer system associated with said volatile latch array ~~non-volatile memory~~, thereby resulting in the transfer of said repairing data to said non-volatile memory.

Claim 17 (currently amended): A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a read circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory;

providing a plurality of columns and rows associated with said non-volatile memory;

associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;

associating a spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and

an error correction coding circuit enabled during an access of a main array associated with said non-volatile memory for correcting a correctable error ~~to thereby correct correctable errors~~ if a particular address corresponds to an address of at least one defective column, wherein said particular address comprises a Y-address ~~corresponding to said at least one defective column or row~~.

Claim 18 (currently amended): A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a read circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, wherein said ~~column repair data is read utilizing a~~ read circuit is linked to a main array associated with said non-volatile memory and an error correction coding circuit linked to said volatile latch array and thereby to a decoder circuit;

providing a plurality of columns and rows associated with said non-volatile memory;

associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;

associating a spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and

wherein said error correction coding circuit is enabled during an access of said main array for correcting a correctable error ~~to thereby correct correctable errors~~ if a particular address corresponds to an address of at least one defective column, wherein said particular address comprises a Y-address ~~corresponding to said at least one defective column or row~~.

Claim 19 (currently amended): A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a read circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, wherein said ~~column repair data is read utilizing a~~ read circuit is linked to a main array associated with said non-volatile memory and an error correction coding circuit linked to said volatile latch array and thereby to a decoder circuit;

a plurality of columns and rows each associated with said non-volatile memory, wherein each of said plurality of associated columns and rows is further associated with a respective I/O terminal;

a spare column associated with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and

said error correction coding circuit is enabled during reading of said repairing data for identifying and repairing ~~to thereby identify and repair~~ defective columns or rows associated with said non-volatile memory ~~regardless of the corruption of said columns or rows~~ despite corruption of the repairing data as read.

Claim 20 (currently amended): A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a read circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory following initialization of a computer system associated with said non-volatile memory, wherein said ~~column repair data is read utilizing a~~ read circuit is linked to a main array associated with said non-volatile memory and an error correction coding circuit linked to said volatile latch array and thereby to a decoder circuit;

a plurality of columns and rows each associated with said non-volatile memory, wherein each of said plurality of associated columns and rows is further associated with a respective I/O terminal;

a spare column associated with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and

said error correction coding circuit is enabled during reading of said repairing data for identifying and repairing ~~to thereby identify and repair~~ defective columns ~~or rows~~ associated with said non-volatile memory ~~regardless of the corruption of said columns or rows~~ despite corruption of the repairing data as read.

Claim 21 (New): The method of claim 1 further comprising the step of:

using a (16,11) Hamming code to associate said at least one spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal.

Claim 22 (New): The method of claim 1 wherein said non-volatile memory is linked to said information array to share a circuit periphery with said non-volatile memory.

Claim 23 (New): The method of claim 1 further comprising the step of:

enabling the error correction coding circuit unconditionally when accessing an information row within said information array to make certain that said repairing data will be correctly obtained.